

Amendments to the Claims

This listing of claims will replace all prior versions and listings in the application:

Listing of Claims:

1. (Currently Amended) A method for designing an integrated circuit, comprising the steps:
receiving data specifying a plurality of interconnects and components of a design of an integrated circuit; and
optimizing the design of the integrated circuit,
wherein data specifying the plurality of interconnects and devices of the integrated circuit is optimized,~~and~~
~~wherein the optimization is based on at least one characteristic chosen from the group consisting of~~ interconnect channel capacities, scalability of interconnect channel capacities ~~or~~ and isochronous interconnect configuration.
2. (Original) The method as described in claim 1, wherein the optimized data is programmed into a self-programmable integrated circuit so as to provide the designed integrated circuit.
3. (Original) The method as described in claim 1, wherein the optimized data is utilized to synthesize an integrated circuit having the specified design.
4. (Previously Presented) The method as described in claim 1, wherein the optimization is further based on at least one characteristic selected from the group consisting of latency or the arrangement of components.

5. (Previously Presented) The method as described in claim 1, wherein a direct connectivity definition, derived from the optimized data, is utilized to synthesize an integrated circuit.
6. (Canceled)
7. (Original) The method as described in claim 1, wherein optimizing is performed without user intervention by an agent.
8. (Previously Presented) The method as described in claim 1, wherein the integrated circuit comprises at least one circuit selected from the group consisting of an application specific integrated circuit (ASIC) and multiple application specific integrated circuits (ASICs).
9. (Original) The method as described in claim 1, wherein interconnects not specified by a user are automatically configured by an agent.

10. (Currently Amended) A self-programmable integrated circuit, comprising:

a processor suitable for performing a program of instructions, the processor accessible via a first interconnect;
at least two components of the integrated circuit, the components communicatively connected via a second interconnect; and
a memory suitable for storing a program of instructions,
wherein the program of instructions configures the processor to optimize the integrated circuit based on heuristic data indicating past utilization of components of the integrated circuit,
wherein, the heuristic data is optimized based on ~~at least one characteristic selected from the group consisting of~~ interconnect channel capacities, scalability of interconnect channel capacities, ~~or~~ and isochronous interconnect configuration.

11. (Previously Presented) The self-programmable integrated circuit as described in claim 10, wherein at least one of the components is selected from the group consisting of a core, functional block or logical block.

12. (Previously Presented) The self-programmable integrated circuit as described in claim 10, wherein the heuristic data includes data indicating amount of data transferred between a first component and a second component over the second interconnect.

13-20. (Canceled)

21. (Previously Presented) The self-programmable integrated circuit as described in claim 10, wherein the heuristic data optimization is further based on at least one characteristic chosen from the group consisting of latency, or the arrangement of components.